Model 652/652A
DATA TRANSMISSION TEST SET

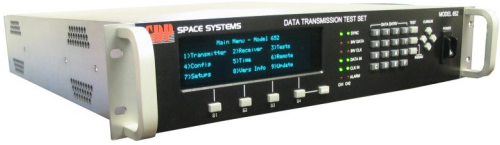
DELTA TELEMETRY SYSTEMS

DATA ACQUISITION

KEY FEATURES

- 2 Independent Data Link Testing Channels
  - Each channel can select between two RS-449 channels & one HSSI channel
  - TTL I/O Optional (MD652A)
  - Bit rates up to 52 Mbps per channel
  - Independent Transmitter and Receiver on each channel
- Measures: Bits, Seconds, Bits in Error, Seconds in Error, Bit Error Rate (instantaneous and average)
- Bit Slip Tests
- TX & RX Frequency Measurement
- 16 PRN Sequence Codes Forward & Reverse
  - 2n-1, n= 5, 7, 9, 11, 15, 20, 23, 31 (Forward or Reverse)
  - User Defined Taps on 31-bit Register.
- Fixed Programmable Data Patterns 8, 16, 32, 64, 128, 256-bit or Dotting
- Internal DDS Frequency Synthesizer or External clock inputs
- IRIG-106 Code Generation and Conversion
- Randomizer / Derandomizer
  - IRIG-106, V.35, V.36
- Remote Control / Monitor: RS232
- 3½" Rack Mount Chassis
- Expansion Slots for Future Options

GENERAL DESCRIPTION



The GDP Model 652 Data Transmission Test Set fills the need for high performance data-link verification and qualification at an affordable price. The user is provided with two totally independent channels, and each channel provides independent transmit and receive functions. This allows for rapid fault isolation and data link characterization. Features such as an internal 6-digit frequency synthesizer and IRIG-106 Bit-Code generator and converter make the Model 652 especially suited to the test and evaluation of data link systems and components.

The Model 652 provides measurement of:

Accumulated Bit Errors, Measured Bit Error Rate, Elapsed Test Time, Accumulated Errored Seconds, Accumulated Bit Count Integrity loss (Bit Slips), Measured Transmit and Receive clock rate.

Operating ease and test flexibility is the result of using microprocessor control to augment high-speed hardware functions. A high contrast vacuum fluorescent display provides setup and test result information in easy-to-use formats.

FUNCTIONAL DESCRIPTION

The unique architecture of the Model 652 provides superior flexibility. A fully programmable frequency synthesizer allows transmit clock generation from 1 bps to 52 Mbps with 6-digit resolution. A flexible interface structure, which provides IRIG-106 code converters for both input and output data, allows the Model 652 to fully support test and evaluation of telemetry processing systems.

The BER (Bit Error Rate) Module, is the major functional element in the Model 650. A microprocessor resident on the BER module controls the BERT transmit and receive circuits through user commands issued from the local front panel or remote control port. Communication between the microprocessor module and the BER module is accomplished using semaphores passed into a dual-port RAM architecture. All high-speed functions are provided by hardware

Functions such as data generation, PRN correlation, error detection and accumulation are performed by hardware. Low speed functions, such as test result accumulation and formatting for the front panel and remote monitoring ports, are provided by the embedded microprocessors.

Expansion slots are provided for addition of options. The Model 652A is available which is the standard MD652 with additional TTL Inputs and Outputs.

APPLICATIONS

DATA LINK TESTING

The Model 652 provides the capability to perform data-link quality analysis and overall system checkout. A single Model 652 provides two independent data transmit and data receive circuits to support loop-back verification of a unit / system under test.

The Model 652 is user programmed for a particular data pattern and bit rate. By utilizing appropriate connection points in the communications system, the entire data link is tested. The Model 652 synchronizes recovered data and test results are made available for user analysis.

DATA ACQUISITION

Model 652/652A
DATA TRANSMISSION TEST SET

GENERAL SPECIFICATIONS

Two Independent Channels

- Each channel provides Independent Transmitter and Receiver
- 1 bps to 52 Mbps NRZ codes
- (26 Mbps for 2X codes)
- I/O Data Types:
- HSSI [Micro-D 50F], RS-449 [DB37F]
- Frequency Display: Measured Receive and Transmit frequency
- Data Pattern Selectable:
  - Forward and Reverse PRN codes:
  - 2 N-1 [N= 7, 9, 11, 15, 20, 23, 31]
  - User selectable Taps
  - Recycle data patterns, programmable 8, 16, 24, 32, 64, 128, 256 bits or Dotting
- IRIG-106 Bit-Codes: NRZ-L/M/S; BiØ-L/M/S
- Data Randomizer / Derandomizer:
  - V.35, V.36 or IRIG-106 RNRZ-L (215-1)

TRANSMITTER

Independently Selectable Data/Clock Outputs, each channel contains:

- HSSI 52 Mbps
- RS-449 35 Mbps (2 output connections per ch)
- TTL 40 Mbps (Optional)

Clock Source:

- External Terminal Timing Input
- Internal Frequency Synthesizer, Six (6) digit-plus-exponent
- Data Perturbations:
- Force output ALL 1s or ALL 0s
- Insert a single error
- Insert a single slip
- Insert bit-error-rate from 1.00 x 10-06 to 5.00 x 10-01
- Insert Gap (Data forced to zero)
- Programmable Data Gap from 1 to 9999 bit times forced to zero and a programmable period of 1 to 9,999,999 bits between gaps.
- Selectable Data Slip after a programmable period of 1 to 9999 bit times

Data Delay (NRZ):

- Tunable from 0 to 650 nsec (in 5 nsec steps)

External 10MHz Reference Clock

- Input: 0 to +10 dBm, ¼ watt max power
- Output: Accuracy 10 ppm

RECEIVER

Input Termination:

- HSSI- 50 Balanced 110 Ohms Line-to-Line
- RS-449– Balanced 120 ohms Line-to-Line
- TTL –75 ohms or 50 ohms (Optional)

Receive Data and Clock, Synchronization:

- Auto Polarity Correction
- Auto-correlation: BER up to 3 x 10 -1.
- Selectable Resynchronization Threshold
- Errors/Second Allowance Threshold: Selectable 0 to 15

Tests:

- Test length from 102 thru 1012 bits
- Total Count since test start: Bits, Bits-in-Error, Seconds, Errored-Seconds, Slips
- Calculations: Bit-Error Rate,
- Average Bit-Error Rate

ANALOG INTERFACE (OPTION)

Transmit Data with level and offset adjust:

- Signal level: 100 mVp-p to 4 Vp-p (50 Ω Load)
- DC offset: Up to +5V or - 5V (Peak signal + Offset + Noise)
- AC Offset
- Bit Rate Jitter

Noise: (Option)

- Internal programmable Eb/No generator
- External Noise Input

LOCAL FRONT PANEL CONTROL

- Power ON/OFF
- Display and Keypad
- Soft Control Keys
- LED Status

MISCELLANEOUS

AC Input:

- 90 to 264 VAC Auto-set
- Single Phase, 47-63 Hz

Size:

- 3.5 (H) x 20 (D) x 17 (W), inches
- Weight: 20 lbs.
- Mounting: 19 inch EIA rack mount

Environment, Operating:

- Temperature: 0 to 40o C
  - 280 C to 600 C Non-Operating
- Relative Humidity: 5 to 95%, no condensation
- Altitude: 0 to 10,000 ft
- Forced-air Cooling

REMOTE CONTROL

- RS-232 Serial Interface (Std)
- IEEE488 Interface (Optional)
- Ethernet - 10/100 Base T (Optional)

ORDERING INFORMATION

MD652-00 Base Unit

OP652-01 TTL I/O

OP652-22 Ethernet Remote Control

OP652-89 Chassis Slides

MD652A Basic Unit with TTL I/O Option

Inquire today to learn more .

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