Model 2365A

DELTA TELEMETRY SYSTEMS

MULTI-CHANNEL TOUCH-SCREEN PCM BIT SYNCHRONIZER

DATA ACQUISITION

KEY FEATURES

- Up to 8-Channels in 4U
- Bit Rate Range:
  - 5 bps to 20 Mbps
  - 5 bps to 40 Mbps (Option)
- Performance within 1 dB of theory
- Loop Bandwidth Settings from 0.01% to 1.6%
  - Extended LBW Range (Option)
- NRZ-L/M/S; BiØ-L/M/S; DM-M/S; MDM-M/S
- Randomizer/Derandomizer
- Descrambler
  - CCITT V.35 / V.36
- Viterbi Decoder
- Frame Pattern Detector
- Input Signal Status
  - Bit Sync and Signal Loss
  - Pattern Detector Status
  - Viterbi Decoder Status
  - Bit Rate Deviation
  - Signal Level
- Signal/Data Quality Status
  - Eb/No Measurement
  - Frame Sync Pattern Error Count (BER)
  - Frame Loss Count
  - Viterbi Error Count (CER)
  - BERT/ PRN BER Measurement
- Date Generator/Simulator
  - Serial
  - QPSK (Option)
- Advanced Lock Detection
- Auto Bit-Rate Scan (Option)
- QPSK/OQPSK/SOQPSK w/ Resequencer (Option)
- Remote Control
  - Ethernet
  - RS-232 or IEEE-488 (Option)
- 7 -inch High Chassis

GENERAL DESCRIPTION

The GDP Model 2365A Multi-Channel PCM Bit Synchronizer houses **up to 8 high-performance bit synchronizer channels** in a 4U chassis. The optimized digital design of this unit affords the highest performance characteristics currently available.

Control and monitoring of all parameters and features is accomplished by way of the local control interface using the built-in keyboard and touch-pad **(optional touch-screen)**. Remote control of the unit is through an Ethernet interface. Remote Control Software is provided which mimics the local front panel on a remote PC.

The bit synchronizers are capable of **maintaining synch at –3 dB Eb/No** with signal levels as low as 0.1 Vp-p. Search acquisition is attainable in less than 50 bits and synchronization is maintained for a period of at least 256 bit periods without a transition.

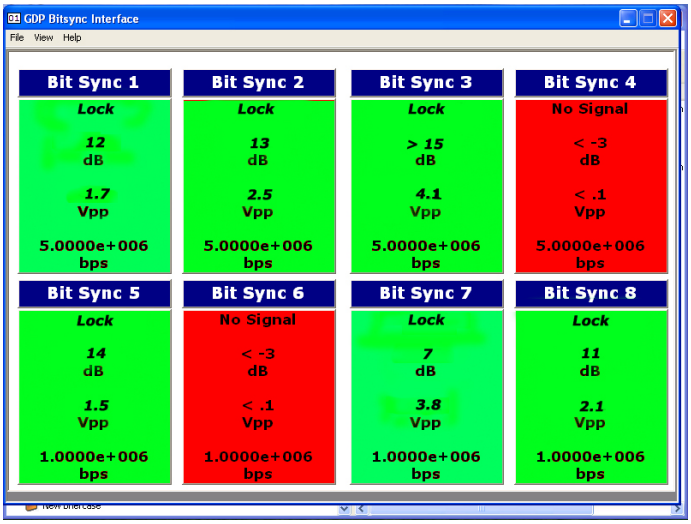
Two Analog inputs are provided per channel. **Optional digital inputs for RS-422 and TTL levels may be included. Each channel presents a variety of standard outputs to support complex system requirements.**

A standard **IRIG 106 randomizer/derandomizer** (forward and reverse) is included as is a CCITT V.35 and V.36 descrambler. A variety of Viterbi decoders are available including R1/2 K7 (Std), R3/4 K7 and R1/3 k7 (please **inquire for other FEC options**). Reed Solomon Decoding is also optional.

The **Pattern Detector** adds an additional level of synchronization assurance by invoking the Frame Pattern Detector. **Automatic Polarity Correction** (APC) may be invoked when using the Pattern Detector.

Data-stream quality is measured and reported to the user as: Eb/No, Frame Synch Pattern BER / Viterbi Decoder CER. A data stream generator / simulator is available to facilitate system testing, and providing a **BERT function**.

An Auto Scan feature is available that causes the bit synchronizers to scan the input for up to 8 pre-selected bit rates, input codes and frame patterns. When an acceptable signal is present, the Bit Synchronizer automatically locks to it and recovers the data and clock. Should this signal drop-out, the bit synchronizer reinitiates the scan sequence.



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DATA ACQUISITION

Model 2365A

MULTI-CHANNEL TOUCH-SCREEN PCM BIT SYNCHRONIZER

GENERAL SPECIFICATIONS

Inputs, Each Bit Sync

- Analog Inputs — 2 Inputs per Bit Sync- 50 Ohms (optional 75Ω) or High Z.
- Digital Inputs — Differential RS-422 and TTL (Optional) [Ask about other configurations]

Performance

- Bit Rate Range — 5 bps to 20 Mbps (40 Mbps Optional)
- Tuning Resolution — X.XXXEN (1≤N≤7)
- Input Levels — 0.1 Vp-p Min., +/- 12 V Max.. (others available)
- DC Offsets — 100% of the input peak-to-peak signal level.
- AC Offset — No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
- Loop Bandwidths — 0.01% to 1.6% (Extended LBW Range Optional)
- Acquisition Range — 2x LBW
- Sync Acquisition Threshold — SNR 0 dB
- Sync Maintenance — SNR –3 dB
- Sync Acquisition — ≤ 50 bits
- Sync Retention — 256 bits without transitions
- Bit Error Rate — ≤1 dB from theory to 40 Mbps

Features

- Input/Output PCM Codes — NRZ-L/M/S; BIØ-L/M/S; DBIØ-M/S; DM-M/S; MDM-M/S
- Randomizer / Derandomizer — IRIG 106 forward and reverse [215-1]
- Descrambler — CCITT V.35 / V.36
- Viterbi Decoder — R 1/2, K 7 with G1/G2 Swap and G2 Invert, (others available)
- Resequencer — QPSK / OQPSK / SOQPSK (Optional)
- Frame Pattern Detector — Up to 64 bits with programmable strategy and Automatic Polarity Correction (APC)
- Auto Scan (Optional) — Up to 8 preset: Bit Rate, Code, Frame pattern per Bit Synchronizer.
- Output Data Polarity — Normal / Inverted.
- Output Clock Phase — 0°, 90°, 180°, 270° to 20
- Mbps; 0°, 180° in the range
- 20 Mbps to 40 Mbps.
- BERT Function (option) — Bit-Error-Rate PRN Generator/Error Detector

Outputs, each Bit Sync Channel

- TTL (Each Channel) - Coded PCM and Clock (Programmable 0°, 90°, 180°, 270°)
- RS422 (Each Channel) - Coded PCM and Clock (Programmable 0°, 90°, 180°, 270°)
- Bipolar Tape Output (Each Channel) - 1Vp-p - Coded PCM
- (Other Output Configurations are available.)
- Lock Status for each channel
- Signal Quality Status: Eb/No, Bit Rate Deviation, BERT / PRN BER or Viterbi CER Measurements

ORDERING INFORMATION

MD2365A-0x Basic Dual Channel Unit (20 Mbps)
x=even # channels. [e.g. 8 Ch unit order MD2365A-08]
OP2365A-01 Bit Rate to 40 Mbps
OP2365A-05 QPSK & OQPSK
OP2365A-06 SOQPSK
OP2365A-07 QPSK & OQPSK & SOQPSK Support
OP2365A-17 Touch-Screen Display/KB & Mouse
OP2365A-40 Special Rear Panel
OP2365A-43 BERT
OP2365A-45 Auto Scan
OP2365A-70 75 ohm
OP2365A-91 Extended Loop Bandwidth Range
OP2365A-92 Reed Solomon Decoder

WHY GDP

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications. Over fifty years of experience, far-ranging expertise, excellent products, and outstanding support make GDP not just a telemetry system supplier, but a partner you can rely on to meet your needs.

Inquire today to learn more .

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