Model 650

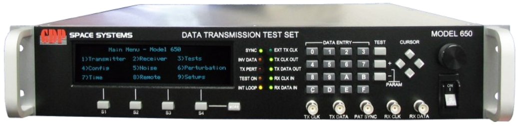
DATA TRANSMISSION TEST SET

DELTA TELEMETRY SYSTEMS

KEY FEATURES

- 1 bps to 36 Mbps Operation (Standard)
    - 1 bps to 50 Mbps Operation (Optional)
- Independent Transmitter and Receiver
- Measures: Bits, Seconds, Bits in Error, Seconds in Error, Bit Error Rate (instantaneous and average)
- Data Symmetry & Bit Slip Tests
- TX & RX Frequency Measurement
- 16 PRN Sequence Codes Forward & Reverse 2n-1, n= 5, 7, 9, 11, 15, 20, 23, 31 (Forward or Reverse) and User Defined Taps on 31-bit Register.
- Fixed Programmable Data Patterns 8, 16, 32, 64, 128, 256-bit or Dotting
- Internal DDS Frequency Synthesizer
    - IRIG Code Generation and Conversion
- Randomizer / Derandomizer (Fwd & Rev)
- IRIG (215-1), 29-1, 211-1, 217-1, 223-1, V.35, V.36
- Convolution Encode / Decode (Optional)
- Low Density Parity Check (LDPC) Generator (Optional)
    - AR4JA Family R= 1/2, 2/3, 4/5 ; K= 1024, 4096
- TTL, Bipolar, RS-422 Signal Interfaces
- Remote Control / Monitor: RS232 (Standard)
    - Ethernet (Optional), IEEE-488 (Optional)
- Internal Noise Source (Optional)
    - Programmable Eb/No and Signal Level
    - Automatic Eb/No Test
- Analog Signal Output Interface (Optional)
- Acquisition Time Test (Optional)
- Jitter Test (Optional)
- Link Delay Test (Optional)

GENERAL DESCRIPTION



The GDP Model 650 Data Transmission Test Set fills the need for data-link verification and qualification at an affordable price. The user is provided with totally independent transmit and receive functions to allow rapid fault isolation and data link characterization. Simulated signal perturbations are created programmably by adding noise, baseline offset, missing bits, bit -rate jitter and varying signal levels. Features such as an internal 6-digit frequency synthesizer and IRIG Code generator and converter make the Model 650 especially suited to the test and evaluation of PCM Telemetry data link systems and components.

The Model 650 provides measurement capability for: Accumulated Bit Errors, Measured Bit Error Rate, Elapsed Test Time, Accumulated Errored Seconds, Errors per Second, Measured Error Symmetry, Accumulated Bit Count Integrity Loss (Bit Slips), Measured Transmit and Receive clock rate.

Operating ease and test flexibility is the result of using microprocessor control to augment high speed hardware functions. A high contrast vacuum fluorescent display provides setup and test result information in easy-to-use formats.

FUNCTIONAL DESCRIPTION

A modular architecture gives the Model 650 superior flexibility. A fully programmable frequency synthesizer allows transmit clock generation from 1 bps to 50 Mbps with 6-digit resolution. A flexible interface structure, which provides IRIG code converters for both input and output data, allows the Model 650 to fully support test and evaluation of telemetry receive, and processing systems.

The BER (Bit Error Rate) Module, is the major functional element in the Model 650. A microprocessor resident on the BER module controls the BERT transmit and receive circuits through user commands issued from the local front panel or remote control port. Communication between the microprocessor module and the BER module is accomplished using semaphores passed into a dual-port RAM architecture.

All high-speed functions such as data generation, PRN correlation, error detection and accumulation are performed by hardware. Low speed functions, such as test data accumulation and formatting for the front panel and remote monitoring ports, are provided by the embedded

APPLICATIONS

DATA LINK TESTING

In a telemetry ground station or in a satellite ground data handling system, the Model 650 provides the capability to perform data-link quality analysis and overall system checkout. A single Model 650 provides independent data transmit and data receive circuits to support loop-back verification of a ground station.

The Model 650 is user programmed for a variety of data patterns and bit rates. By utilizing appropriate connection points in the communications system, the entire data link is tested from antenna through bit synchronizer. Recovered data is synchronized by the Model 650 and test results are accumulated for user analysis.

BIT SYNCHRONIZER TESTING

The Model 650 provides high performance functionality and ease-of-use in a single package. Using the internal (option) or external noise source with the adjustable Eb/No setup, greatly simplifies Bit Sync Testing. These features coupled with GDP VI Software make the Model 650 an excellent addition to any telemetry system or Bit Synchronizer Test Station.

Model 650

DATA TRANSMISSION TEST SET

GENERAL SPECIFICATIONS

Operation:

- Independent Transmitter and Receiver
- 1 bps to 36 Mbps NRZ codes Standard
- (17.5 Mbps for 2X codes) Standard
- 1 bps to 50 Mbps NRZ codes Optional
- (30 Mbps for 2X codes) Optional
- TTL-50 Mbps, Bipolar-40 Mbps, RS-422-40 Mbps
- Frequency Display:
- Receive and Transmit Bit Rate, Measured

Input Termination:

- High Z / Low-Z on TTL & Bipolar

Data Pattern Selectable:

- Forward and Reverse PRN codes:
- 2 5-1, 2 7-1, 29-1, 211-1, 215-1, 217-1, 219-1, 220-1, 221-1, 223-1, 225-1, 231-1, User selectable Taps
- Recycle data patterns, programmable
- 8, 16, 24, 32, 64, 128, 256 bits or Dotting pattern
- IRIG Bit-Codes:
- NRZ-L/M/S; BiØ-L/M/S; DM-M/S

Data Randomizer / Derandomizer:

- V.35, V.36 or Fwd/Rev RNRZ-L 2N-1(N=15 [IRIG-STD 106], 9, 11, 17, 23)

Convolutional Encoder (Viterbi Decoder) (Option):

- Rate ½ ; K 7
- Selectable convolution order and polarity

Low Density Parity Check (LDPC) Generator (Option)

- AR4JA Family R= 1/2, 2/3, 4/5 ; K= 1024, 4096 [Refer to IRIG-106 Apx R]

TRANSMITTER

Data/Clock Outputs:

- Transmit I-and Q (Option)-Data
- Transmit Clock

Clock Input:

- External Transmit Clock - Selectable

Transmit Timing:

- Internal Frequency Synthesizer
- Six (6) digit-plus-exponent

Data Perturbations:

- Force output ALL 1s or ALL 0s
- Insert a single error
- Insert a single slip
- Insert bit-error-rates from 1.0E-06 to 0.5
- Insert Gap
- Selectable data slip up to 9999 bit times
- Selectable data gap up to 9999 bit times
- Bit Rate Jitter (Option)
- AC Base-line Variation (w/ Analog Option)
- Signal Amplitude Modulation (w/ Analog Option)

RECEIVER

Receive Data and Clock, Synchronization:

- Auto Polarity Correction
- Auto-correlation BER up to 3 x 10 -1.
- ReSynch Threshold, Selectable
- Error Allowance Threshold

Tests:

- Test length from 102 thru 1012 bits
- Total Count since test start:
- Bits, Bits-in-Error, Seconds, Errored-Seconds, Slips
- Calculations:
- Bit-Error Rate, Symmetry, Average Bit-Error Rate
- Sync Acquisition (Option)
- Data Link Delay (Option)
- BER vs Eb/No Performance
- Jitter Performance

ANALOG INTERFACE (OPTION)

Transmit Data with level and offset adjust:

- Signal level: 100 mVp-p to 4 Vp-p (50 Ω Load)
- DC offset: Up to +5V or - 5V (Peak signal + Offset + Noise)
- AC Offset
- Bit Rate Jitter

Noise: (Option)

- Internal programmable Eb/No generator
- External Noise Input

LOCAL FRONT PANEL CONTROL

- Power ON/OFF
- Display and Keypad
- Soft Control Keys
- LED Status and Test Points

MISCELLANEOUS

AC Input:

- 90 to 264 VAC Auto-set
- Single Phase, 47-63 Hz

Size:

- 3.5 (H) x 20 (D) x 17 (W), inches
- Weight: 20 lbs.
- Mounting: 19 inch EIA rack mount

Environment, Operating:

- Temperature: 0 to 40o C
- Relative Humidity: 5 to 95%, no condensation
- Altitude: 0 to 10,000 ft
- Forced-air Cooling

REMOTE CONTROL

- RS-232 Serial Interface (Std)
- IEEE488 Interface (Optional)
- Ethernet - 10/100 Base T (Optional)

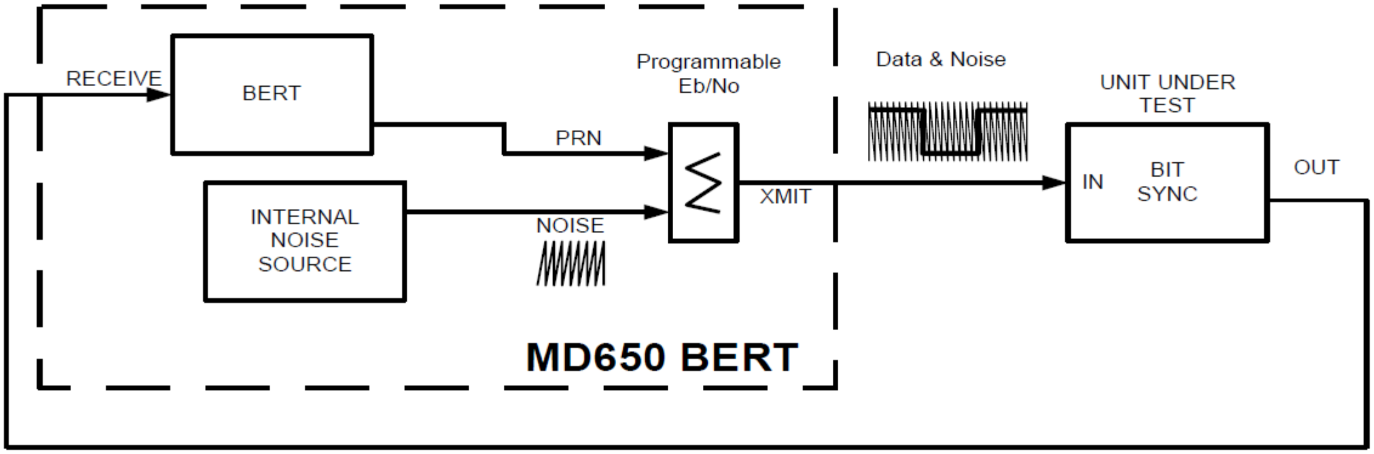
ORDERING INFORMATION

MD650-00 Base Unit
OP650-21 IEEE Remote Control
OP650-22 Ethernet Remote Control
OP650-40 Special I/O
OP650-62 Extended Bit Rate 36 to 50 Mbps
OP650-65 Internal Noise Source
OP650-66 Sync Acquisition Test
OP650-67 Jitter Test
OP650-68 Delay Measurement
OP650-69 LDPC Generator
OP650-70 75 Ohm I/O Impedance
OP650-89 Chassis Slides
OP650-VI Virtual Interface Software

Model 650-65

MODEL 650 OPTION: INTERNAL NOISE SOURCE

OP650-65: DATA LINK ANALYZER INTERNAL NOISE OPTION



Including Noise and Analog output functionality in the Model 650 adds a layer of capability that allows testing of bit synchronizers and data links to a higher level. Real-World performance of a system is more fully characterized under the test conditions provided by this option.

SPECIFICATIONS

Noise:

- White Gaussian Noise
- Eb/No (Programmable): -3 dB to 15.9 dB (0.1 dB increments)
- Automatic Eb/No Settings from Front Panel (No Calculations or Measuring Required)
- Absolute Accuracy: Better than ±0.5 dB (0.1 dB typical)
- All Digital Design
- Repeatable Results
- Easy Bit Synchronizer BER Testing to IRIG106 Theoretical Curves

Output Level:

- 0 to 4 Vp-p into 50 Ohms
- Adjustable Output Signal Level: 0.1 Vpp Steps
- Fixed or AM Modulated Output Signal Level
- Amplitude Modulation Level: 0 to 100% of Peak Signal
- Amplitude Modulation Frequency: 0 to 0.1% of Bit Rate in 0.01% Steps

Baseline Offset:

- Adjustable Static Offset Level: ± 100% Peek Signal Level
- Adjustable Dynamic Offset Rate: 0 to 0.1% of Bit Rate (0.01% Resolution)

Model 650-69

MODEL 650 OPTION: LOW DENSITY PARITY CHECK GENERATOR

Overview:

This LDPC option provides the model 650 BERT with the facility to generate data streams that comply with the requirement outlined in Appendix R of the IRIG 106 Telemetry Standard. The LDPC code is a linear block code that maps k information bits with a code word of n bits.

The LDPC coding scheme does not guarantee enough bit transitions to allow the maintenance of synchronization in receiving devices (bit synchronizers). Therefore, a 28-1 PRN [x8 + x7 + x5 + x3 + 1] is multiplied against the information block. The randomizer is reset to all 1s at the start of each code block.

Furthermore, an Appended Synchronization Pattern is applied to the start of the code block to aid in identifying the start of the block and to assist in the resolution of phase ambiguities. The randomization process is not applied to the synchronization pattern.

Encoding:

Code Rate =1/2, Information Block Size = 1024, M = 512

Code Rate =1/2, Information Block Size = 4096, M = 2048

Code Rate =2/3, Information Block Size = 1024, M = 256

Code Rate =2/3, Information Block Size = 4096, M = 1024

Code Rate =4/5, Information Block Size = 1024, M = 128

Code Rate =4/5, Information Block Size = 4096, M = 512

Synchronization:

The Appended Synchronization Pattern is made up of groups of 64 bits. The number of these groups is dependent upon the size of the Information Block k. Where k = 1024-bits, a single group of 64 ASP bits is applied. When k = 4096-bits, 256 ASP bits are applied as four 64-bit sequences.

The 64-bit ASP is fixed at ‘FCB88938D8D76A4F’ hex. The 256-bit pattern contains one inverted 64-bit sequence [PPpP] where ‘P’ represents the normal bit pattern and ‘p’ is the inverted pattern. The transmitted data stream begins with the left most bit of the synchronization pattern.

Bandwidth Expansion:

Convolution encoding expands the data rate of the encoded stream by the inverse of the Rate factor. E.g. Rate 1/2 convolution encoding doubles the transmitted data rate.

The Bandwidth Expansion of an LDPC data stream is further complicated by the addition of the ASP.

The Expansion Factors are as follows:

Rate 1/2 = 33/16; Rate 2/3 = 25/16; Rate 4/5 = 21/16.

Resultant Bit Rate = Baseband Rate * Rate Factor

Model 650-VI

MODEL 650 OPTION: LOW DENSITY PARITY CHECK GENERATOR

The Virtual Interface (VI) Software for the Model 650 provides an easy to use intuitive Graphic User Interface on a personal computer.

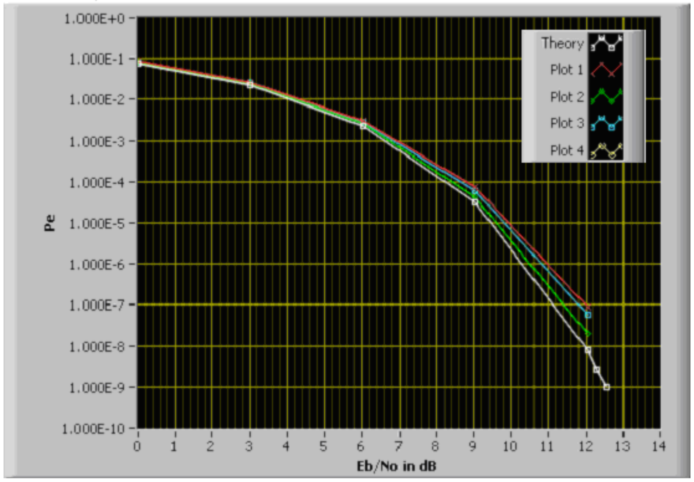
All operational parameters needed to control the Model 650 to accomplish a test are entered into easily understood dialog windows. Once all parameter settings are made, a simple click of a soft button transfers all setup information to the BERT.

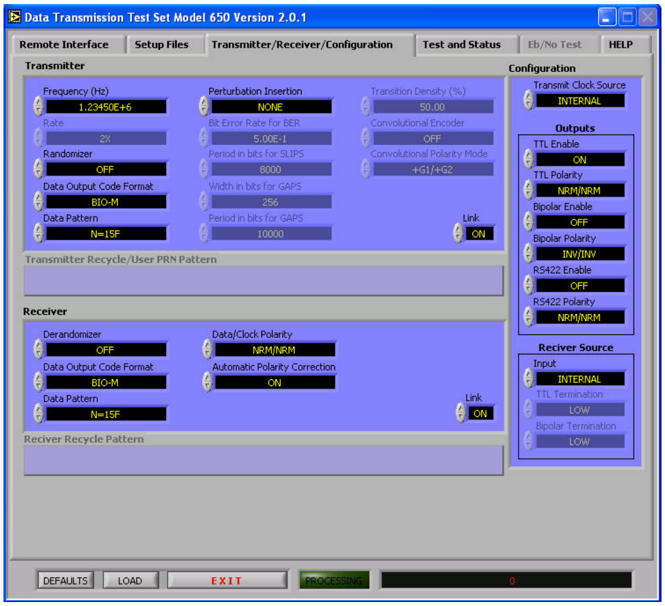
All remote control interfaces, which are available on the Model 650 are supported by the VI. Complex system arrangements consisting of multiple components, provided by GDP Space Systems, are controlled using the bussable interface structures (IEEE-488 or Ethernet) and the appropriate VI software for each unit.

Test results are gathered by the OP650-VI software and presented in a format easily interpreted by the user. A test result log-file may be designated by the user into which all accumulated test result data is stored for use by other software. This data file is recorded as ASCII, comma delimited information making it useful for direct inclusion in written reports.

If the Model 650 includes the Noise option (OP650-65), automatic bit synchronizer and data link testing is made possible, which results in a complete family of noise performance curves. The time consuming task of calculating values of noise and signal levels as well as making settings to filters is automatically performed by the Model 650. The OP650-VI takes full advantage of the features of the Model 650 to provide highly understandable and comprehensive test results.

Pe versus Eb/No for NRZ PSK





Transmitter

Frequency (Hz): 1.23450E+6
Rate: 2X
Randomizer: OFF
Data Output Code Format: BIO-M
Data Pattern: N=15F
Perturbation Insertion: NONE
Bit Error Rate for BER: 5.00E-1
Period in bits for SLIPS: 8000
Width in bits for GAPS: 256
Period in bits for GAPS: 10000
Transition Density (%): 50.00
Convolutional Encoder: OFF
Convolutional Polarity Mode: +G1/+G2
Link: ON

Receiver

Derandomizer: OFF
Data Output Code Format: BIO-M
Data Pattern: N=15F
Data/Clock Polarity: NRM/NRM
Automatic Polarity Correction: ON
Link: ON

Configuration

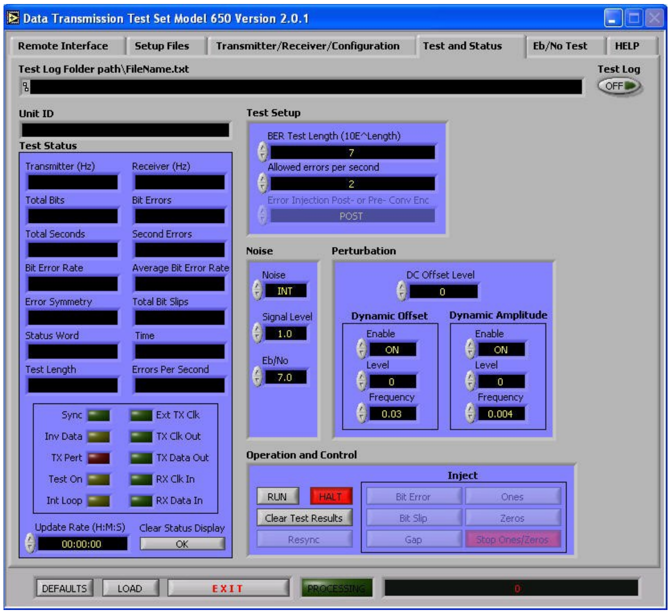
Transmit Clock Source: INTERNAL

Outputs

TTL Enable: ON
TTL Polarity: NRM/NRM
Bipolar Enable: OFF
Bipolar Polarity: INV/INV
RS422 Enable: OFF
RS422 Polarity: NRM/NRM

Reciver Source

Input: INTERNAL
TTL Termination: LOW
Bipolar Termination: LOW



Update Rate (H:M:S): 00:00:00

Test Setup

BER Test Length (10E^Length): 7
Allowed errors per second: 2
Error Injection Post- or Pre- Conv Enc: POST

Noise

Noise: INT
Signal Level: 1.0
Eb/No: 7.0

Perturbation

DC Offset Level: 0

Dynamic Offset

Enable: ON
Level: 0
Frequency: 0.03

Dynamic Amplitude

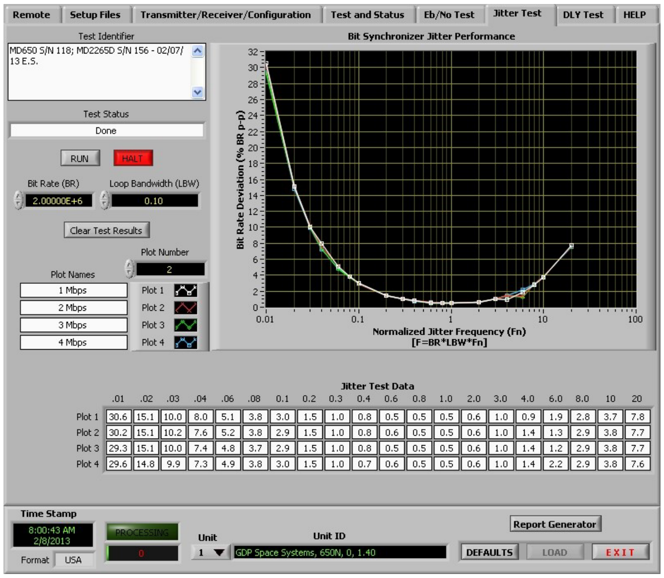
Enable: ON
Level: 0
Frequency: 0.004

Model 650

MODEL 650 OPTION: VIRTUAL INTERFACE SOFTWARE

JITTER SUSCEPTIBILITY TESTING

All PCM bit synchronizers are susceptible to bit-rate jitter (FM). Jittery signals are common from multiplexers and other equipment that store and forward PCM. The optional Jitter Test function provides an automatic mechanism to perform a jitter performance test on a PCM bit synchronizer. This test results identifies the performance limitation of a PCM bit synchronizer when the input signal is corrupted by bit rate (FM) variations. The test process produces a data bit stream that is frequency modulated at specific frequencies and automatically adjusts the amplitude of the modulation until the bit synchronizer begins to produce an output that contains errors. The test results are presented as a series of normalized frequencies with associated jitter amplitudes. The gathered test results are plotted to clearly reveal the bit synchronizer performance in the presence of a jittery input signal. Additionally, the true Loop Bandwidth setting of the bit synchronizer is indicated by the test results.



Test Identifier: MD650 S/N 118; MD2265D S/N 156 - 02/07/13 E.S.

Test Status: Done

Bit Rate (BR): 2.00000E+6

Loop Bandwidth (LBW): 0.10

Plot Number: 2

Plot Names	
1 Mbps	Plot 1
2 Mbps	Plot 2
3 Mbps	Plot 3
4 Mbps	Plot 4

Jitter Test Data

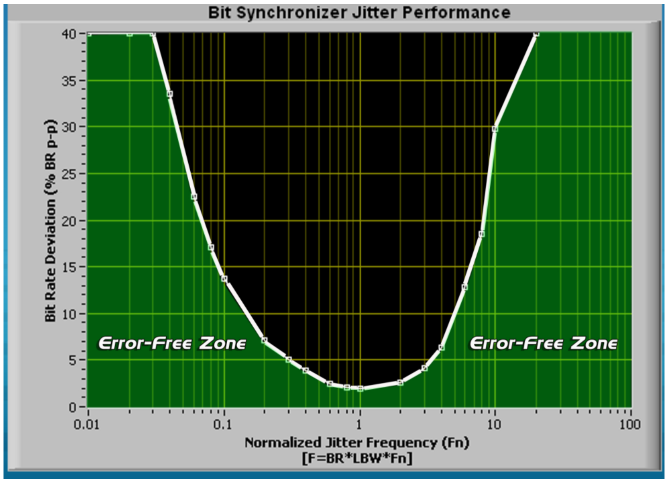
	.01	.02	.03	.04	.06	.08	0.1	0.2	0.3	0.4	0.6	0.8	1.0	2.0	3.0	4.0	6.0	8.0	10	20
Plot 1	30.6	15.1	10.0	8.0	5.1	3.8	3.0	1.5	1.0	0.8	0.5	0.5	0.5	0.6	1.0	0.9	1.9	2.8	3.7	7.8
Plot 2	30.2	15.1	10.2	7.6	5.2	3.8	2.9	1.5	1.0	0.8	0.6	0.5	0.5	0.6	1.0	1.4	1.3	2.9	3.8	7.7
Plot 3	29.3	15.1	10.0	7.4	4.8	3.7	2.9	1.5	1.0	0.8	0.5	0.5	0.5	0.6	1.0	1.4	1.2	2.9	3.8	7.7
Plot 4	29.6	14.8	9.9	7.3	4.9	3.8	3.0	1.5	1.0	0.7	0.6	0.5	0.5	0.6	1.0	1.4	2.2	2.9	3.8	7.6

Time Stamp: 8:00:43 AM 2/8/2013

Format: USA

Unit: 1

Unit ID: GDP Space Systems, 650N, 0, 1.40

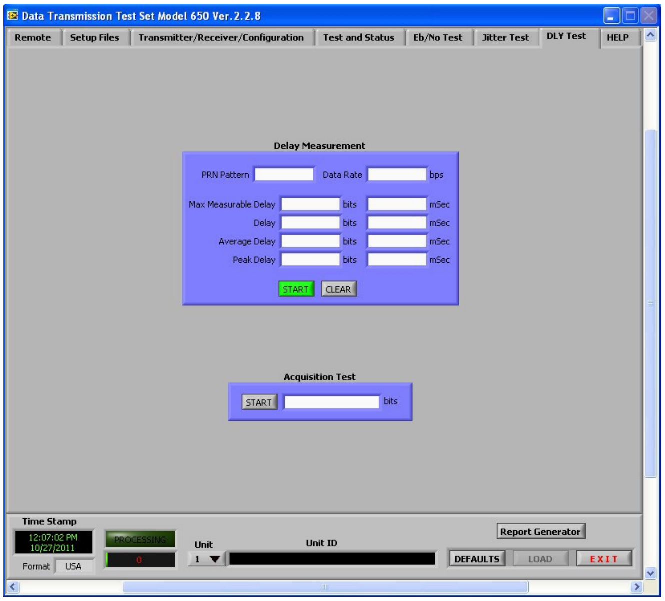


LINK DELAY (LATENCY) TESTING

The Virtual Interface GUI presents a clear method of collecting and displaying the results of the MD650 Delay Test. The measured delay (latency) is presented in terms of bits and time.

ACQUISITION TIME MEASUREMENT

The MD650 measures and the VI GUI presents the measurement of the number of bit periods required for a bit synchronizer



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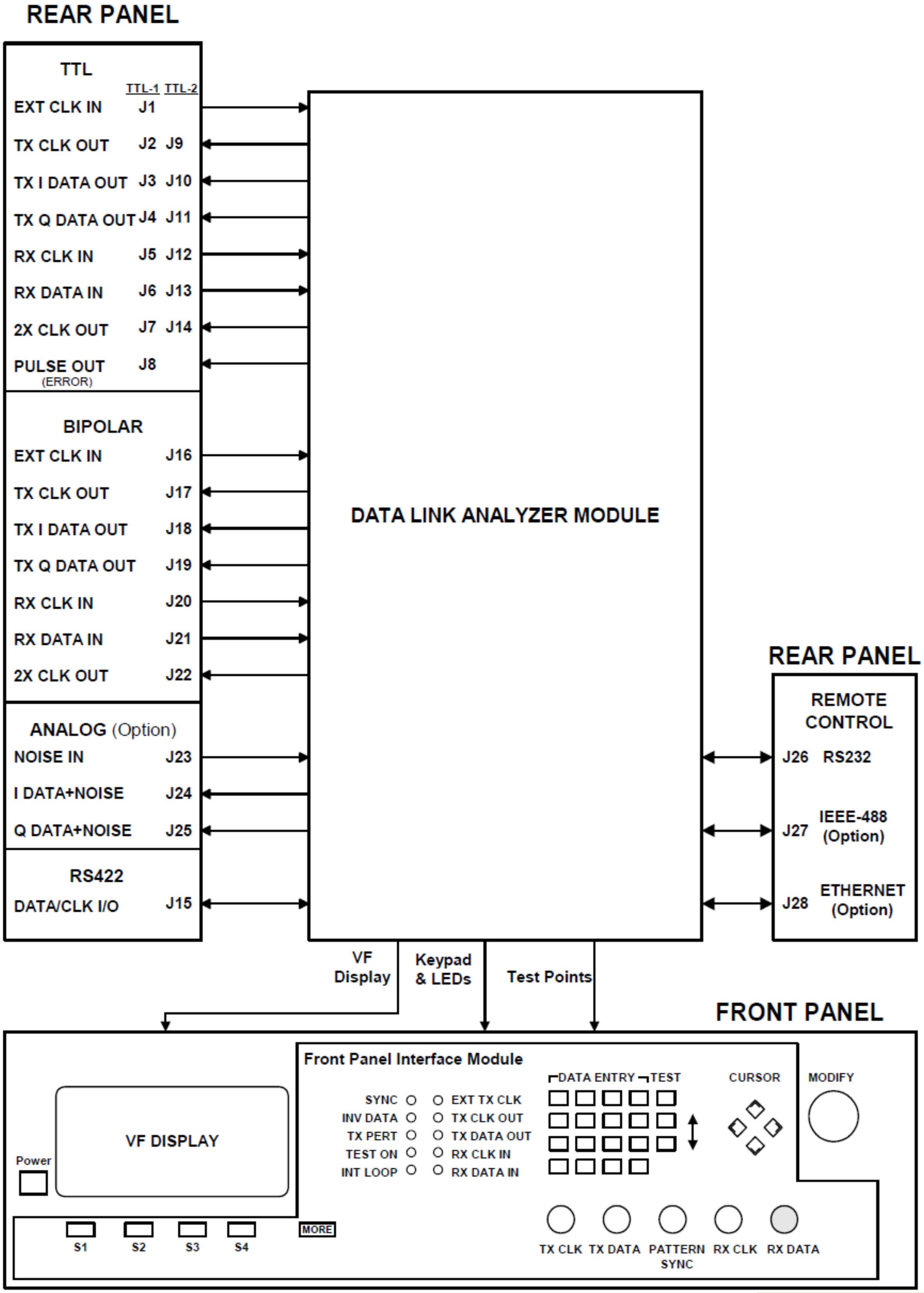
Unit: 1

Model 650

DATA TRANSMISSION TEST SET



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